Bug Localization Techniques for Effective Post-Silicon Validation

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ABSTRACT

Post-silicon validation is used to detect and fix bugs in integrated circuits and systems after manufacture. Due to sheer design complexity, it is nearly impossible to detect and fix all bugs before manufacture. Existing post-silicon validation methods barely cope with today's complexity. New techniques are essential to minimize the effects of bugs and design flaws going forward. This talk will focus on two recent techniques, QED and IFRA, that can overcome significant challenges associated with a very crucial step in post-silicon validation: bug localization in a system setup. We demonstrate the effectiveness of these techniques using results from quad-core Intel Core i7 hardware platforms and Intel Nehalem processors, and using actual examples of "difficult" bugs that occurred in complex SoCs.

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