Robust Systems for Scaled CMOS and Beyond

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Acknowledgment: Students & Collaborators

Robust System Design

Perform correctly despite complexity & disturbances

- Complexity: detect & fix design bugs
- CMOS reliability limits: tolerate errors
- Beyond silicon-CMOS: imperfection-immune logic

What's New ?

- Existing approaches: inadequate, expensive

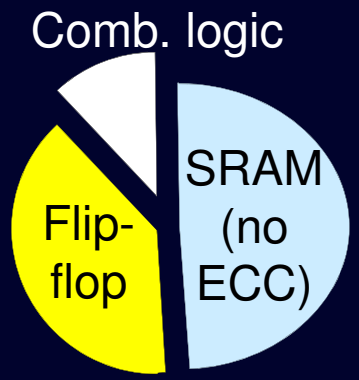
	Traditional Thinking	New approach
Design bugs	Pre-silicon	**Post-silicon**
Reliability failures	Avoid	**Tolerate at low cost**
Beyond silicon-CMOS	Material processing	**Imperfection-immune design**

Outline

- Introduction
- CMOS reliability limits: tolerate errors
- Beyond silicon-CMOS: imperfection-immune logic
- Conclusion

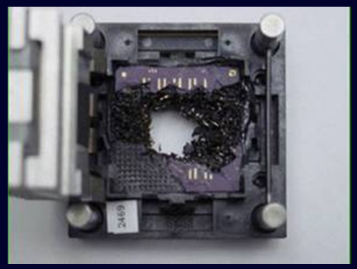
Technology Reliability Challenges

- System soft error rates increasing
  - **Fatal** flip-flop errors



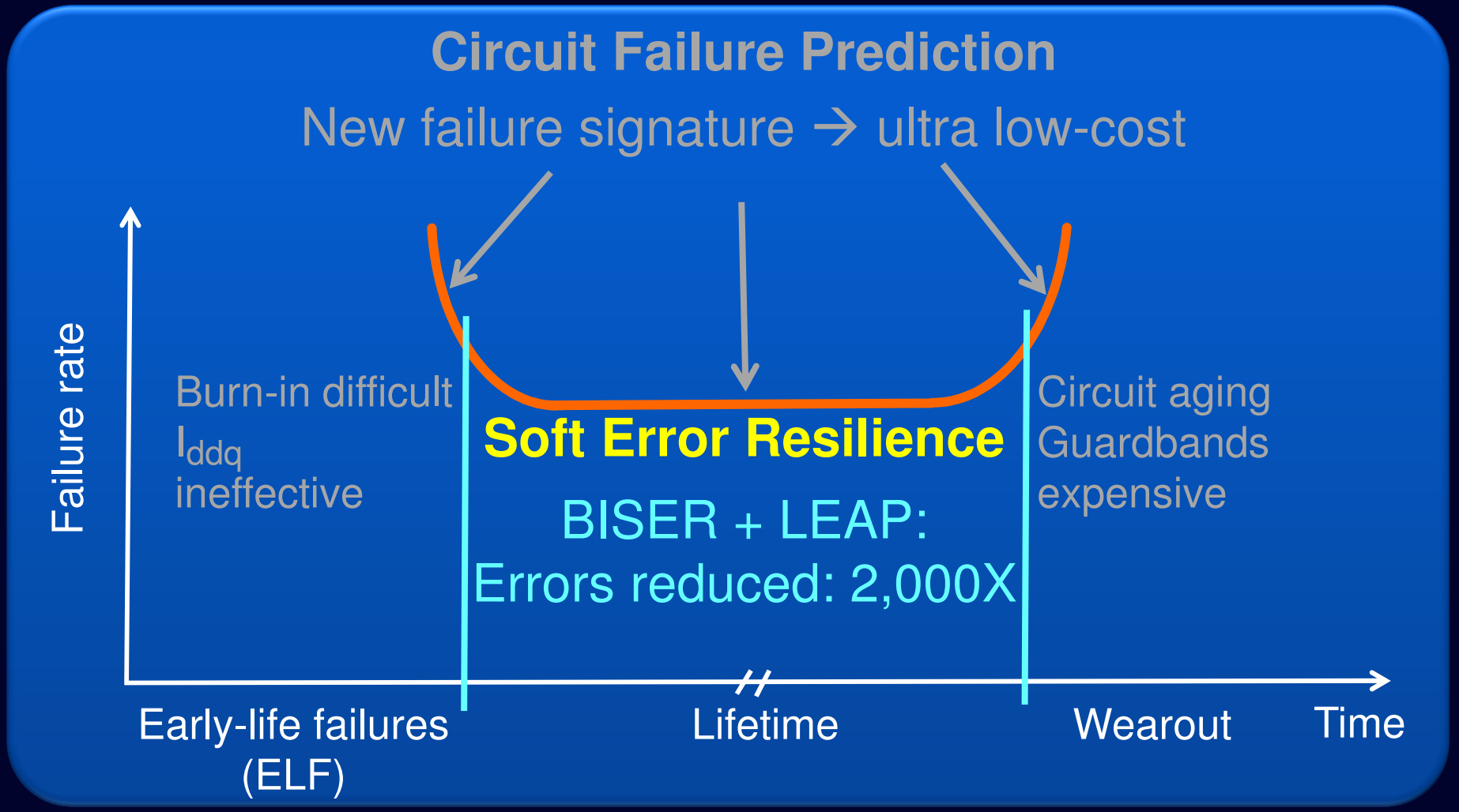
Soft error rates

- Early-life failures (ELF)
  - Burn-in: difficult, expensive



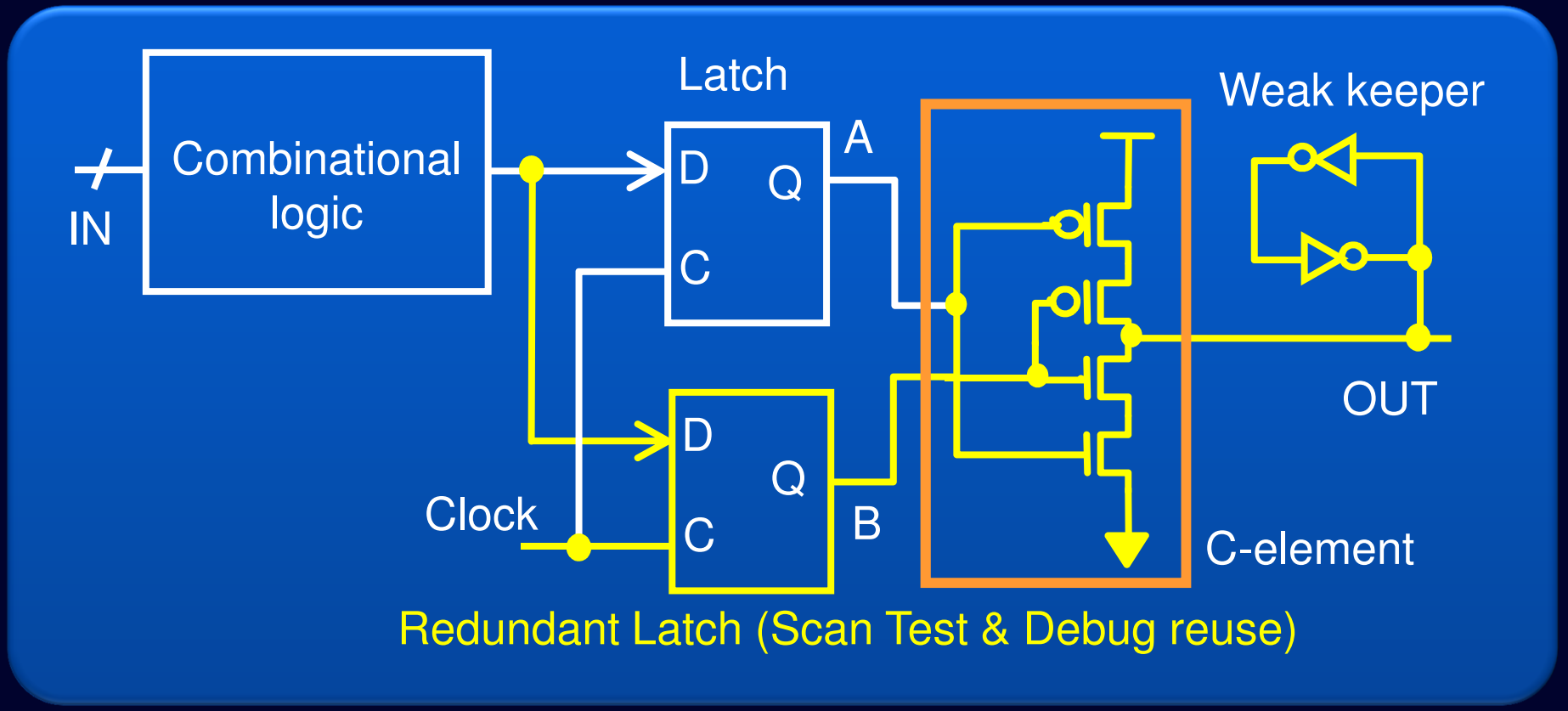
- Circuit aging & variations
  - Worst-case guardbands expensive

Low-Cost Resilience



Software-orchestrated global optimization a MUST

BISER: Built-In Soft Error Resilience

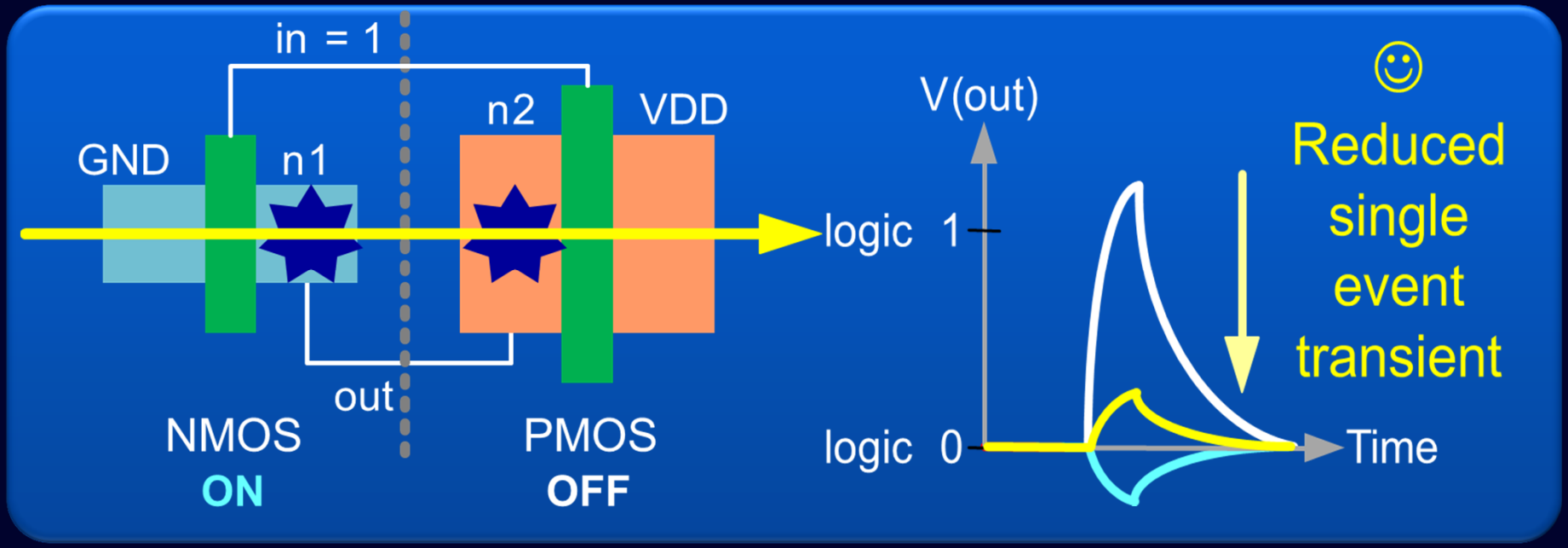


45nm: up to 1,000X fewer errors vs. D-flip-flop

Single Error Assumption Inadequate

- Single event **multiple** upsets increasing

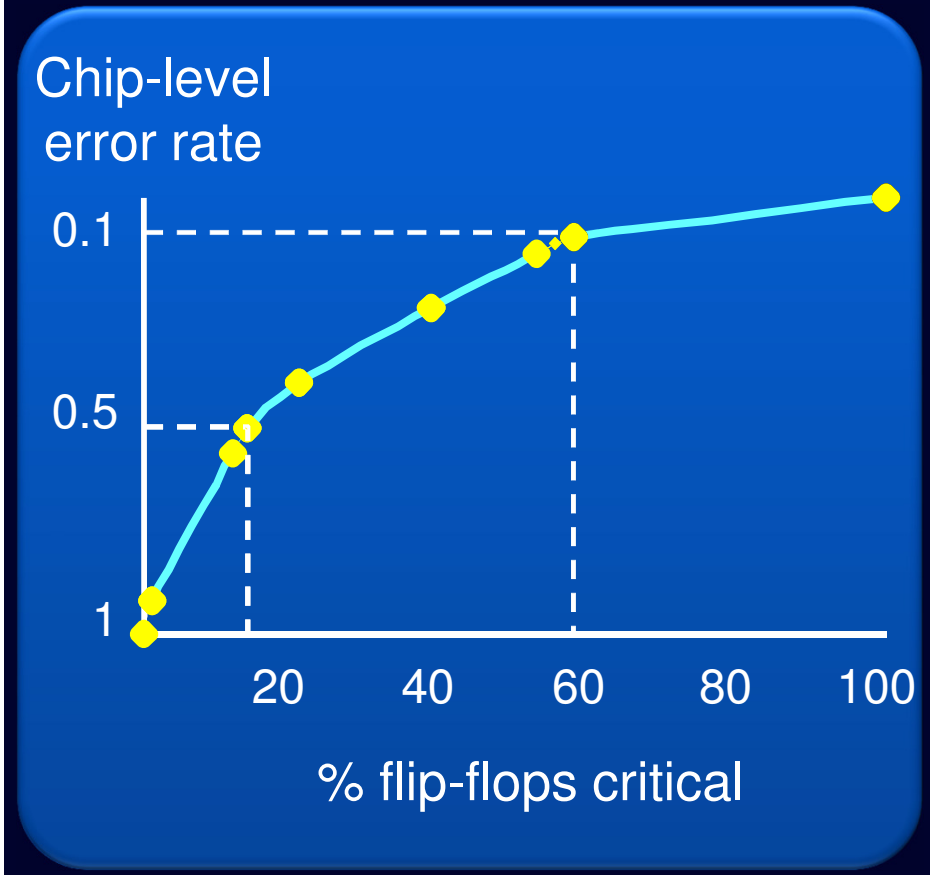
LEAP: Layout by Error Aware transistor Positioning



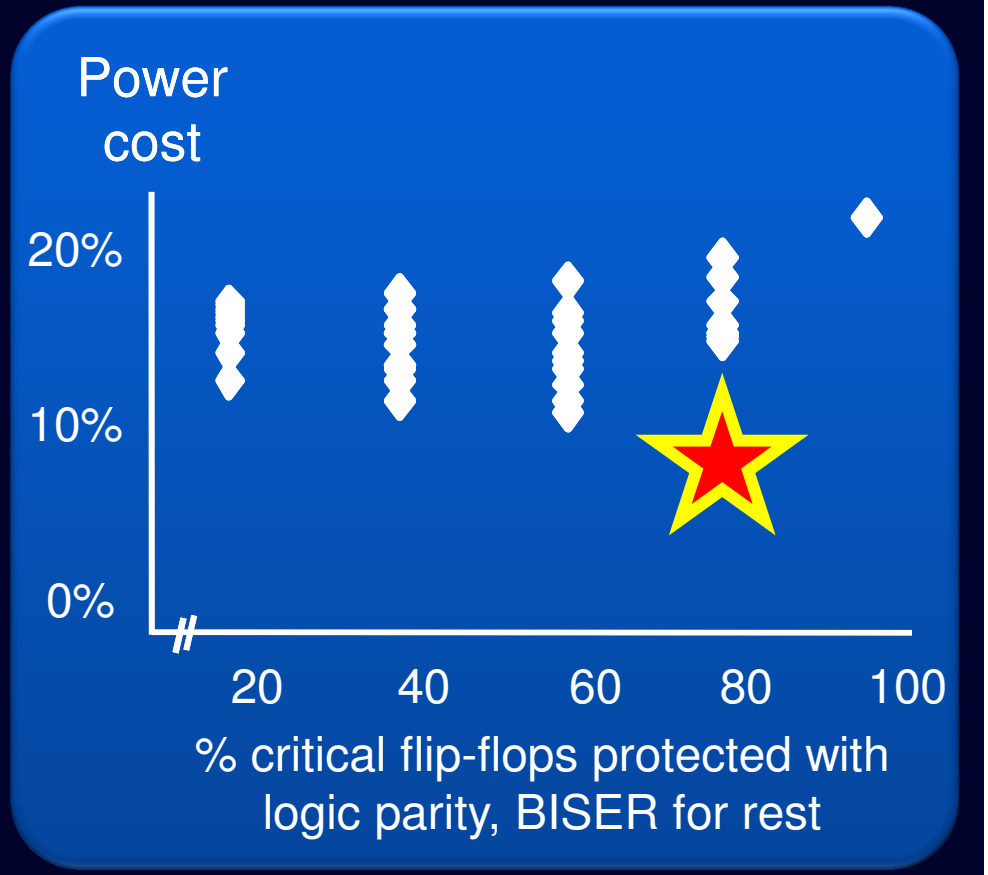
2,000X fewer errors vs. D-flip-flop

Optimized Resilience Essential

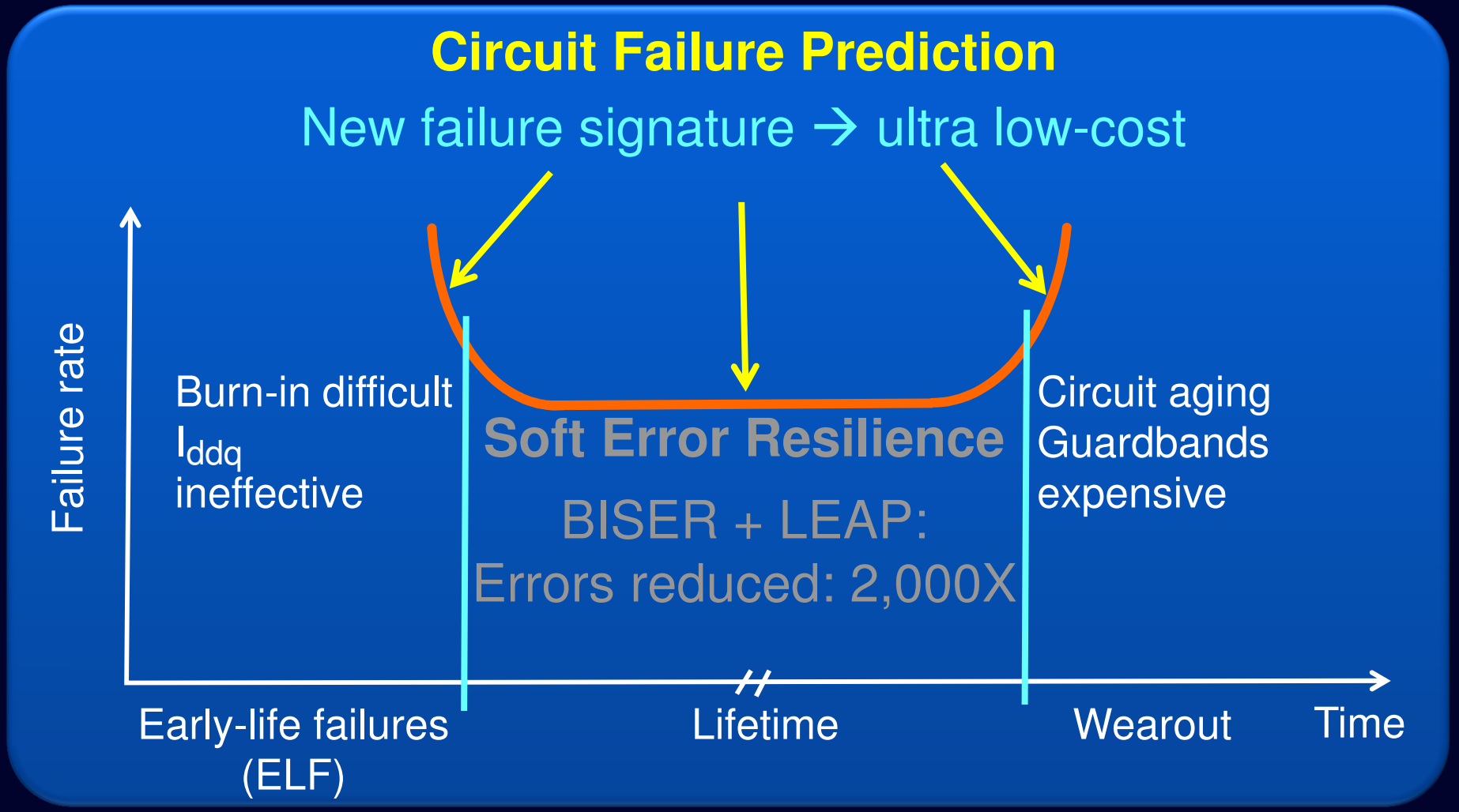
Select application-critical flip-flops



Optimize for cross-layer resilience



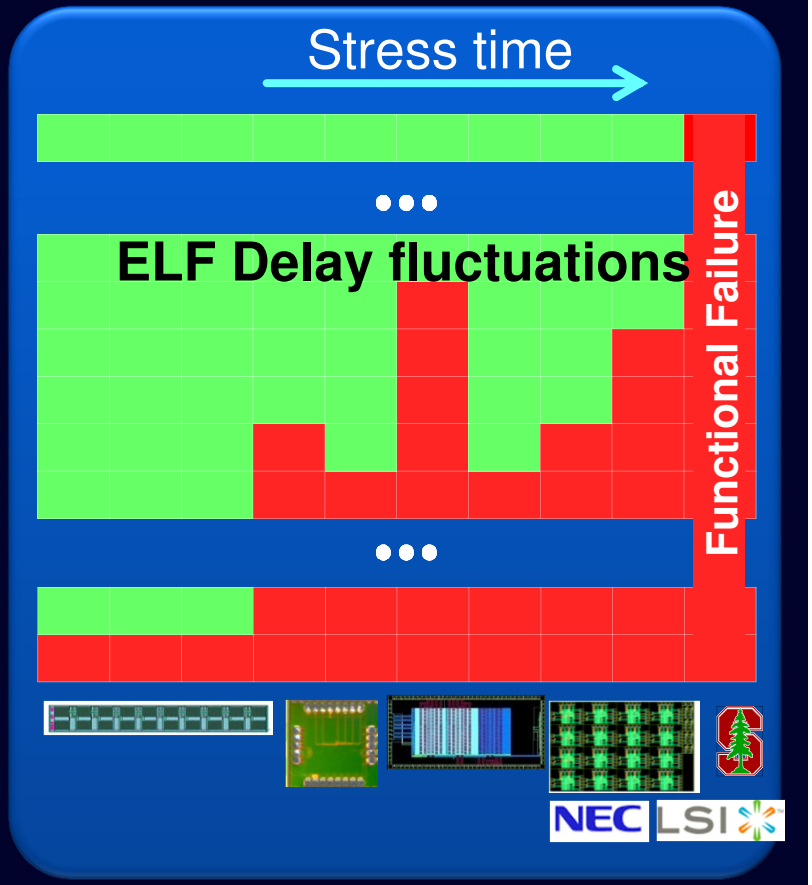
Low-Cost Resilience



Software-orchestrated global optimization a MUST

New Gate-Oxide ELF Signature

- **Delay fluctuations over time**
  - Before functional failure
- Demonstrated: 45, 32nm
  - 28, 22, 15nm in progress
- Enables
  - On-line failure prediction



On-line Failure Prediction

Failure Prediction	Error Detection
Before errors appear	After errors appear
+ No corruption	– Corrupt data & states
+ Low cost	– High cost
+ Self-diagnostics	– Limited diagnostics

How ?

On-line self-test and diagnostics

On-Line Self-Test and Diagnostics

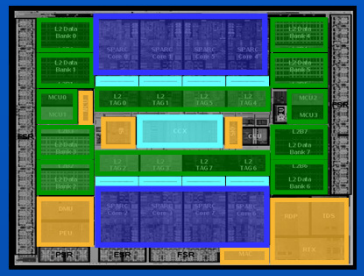
On-line self-test & diagnostics

CASP

High on-line test coverage

No visible system downtime

OpenSPARC T2 SoC



Uncore very important

1% power, 1% area, 3% performance impact

Ultra low-cost

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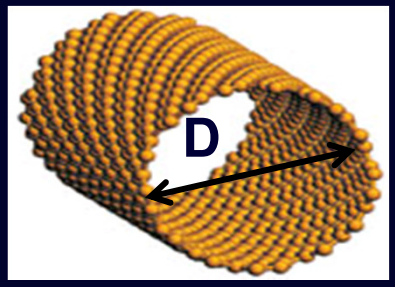
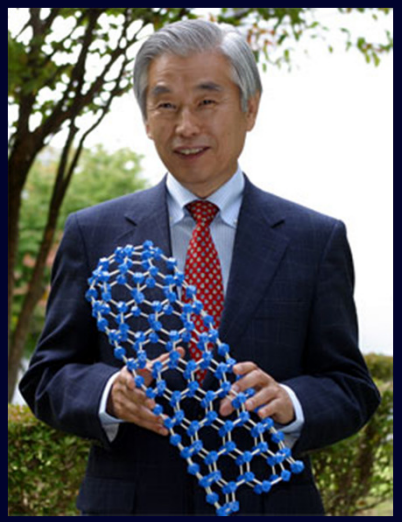
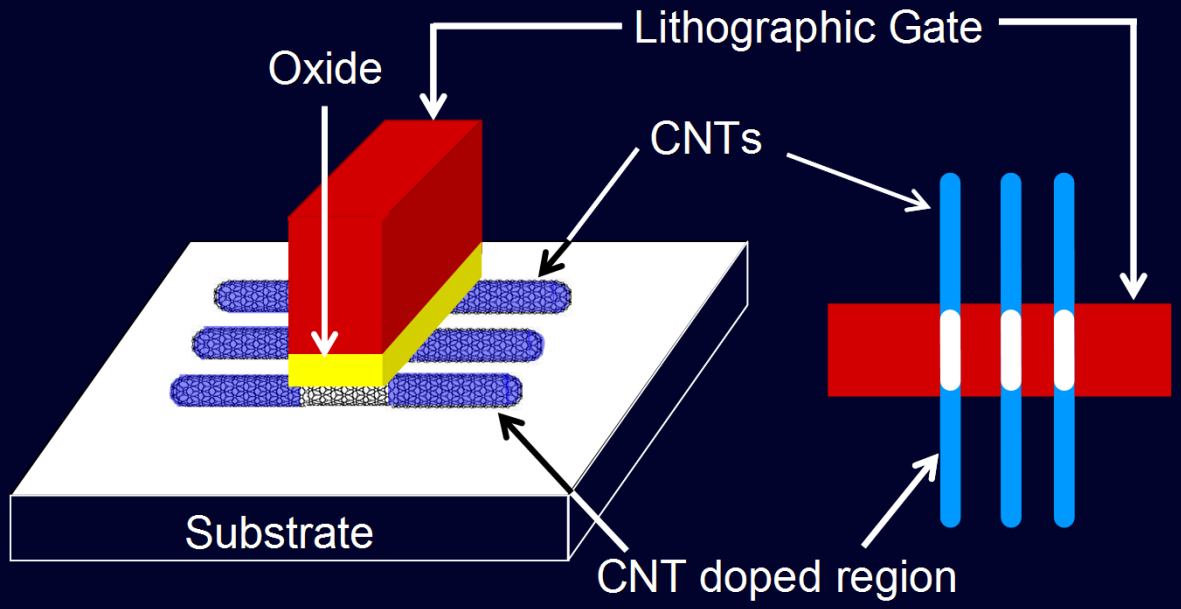
Carbon Nanotube FET (CNFET)

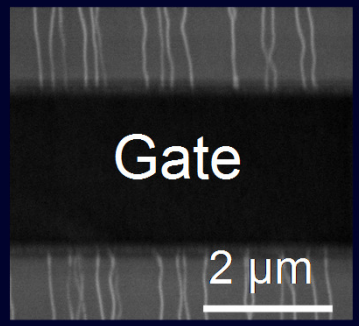


Carbon Nanotube (CNT)
Diameter (D) : 0.5 - 3 nm

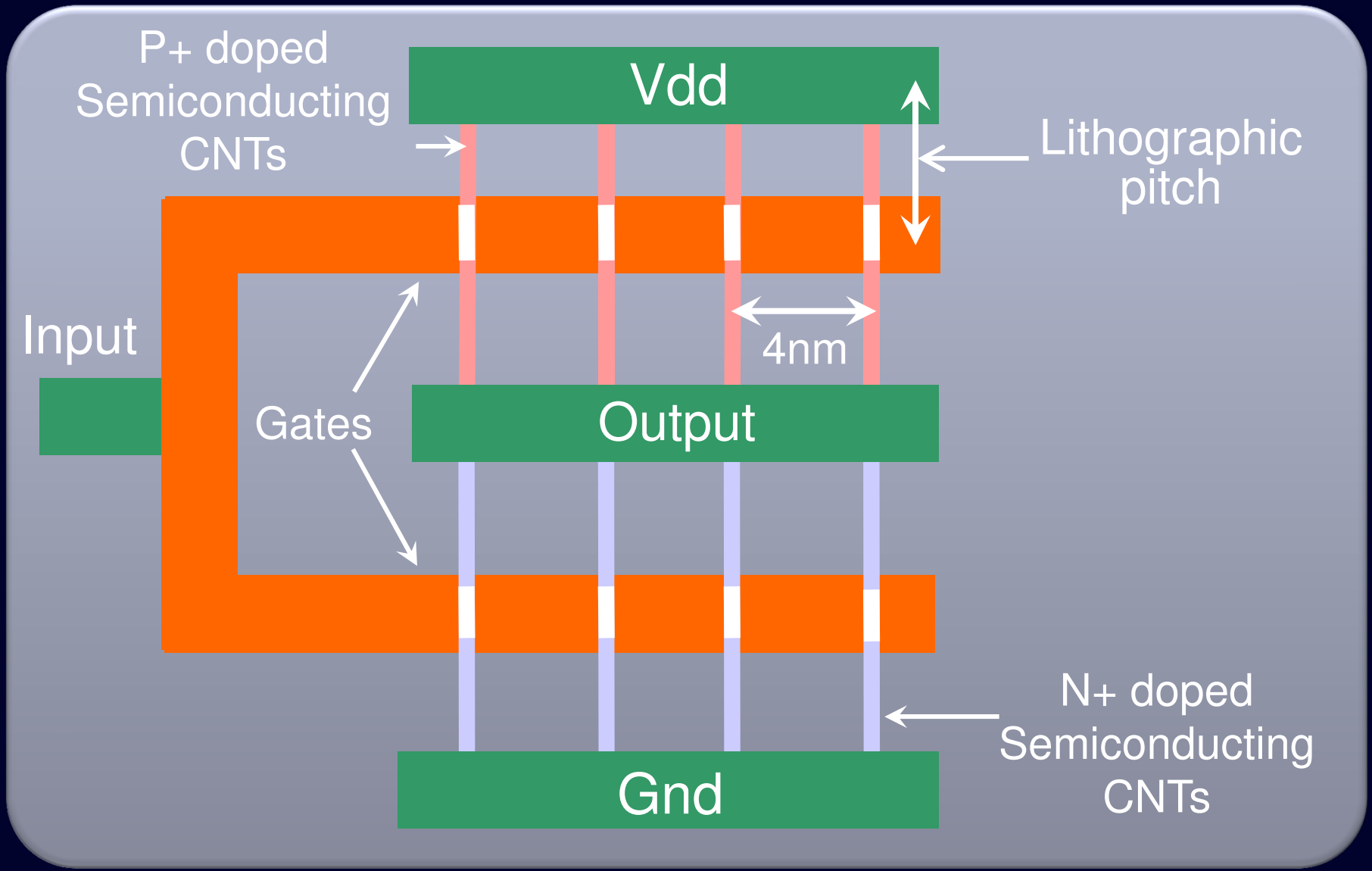


S. Iijima



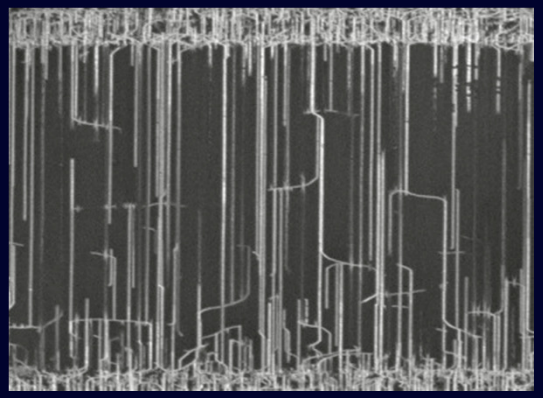


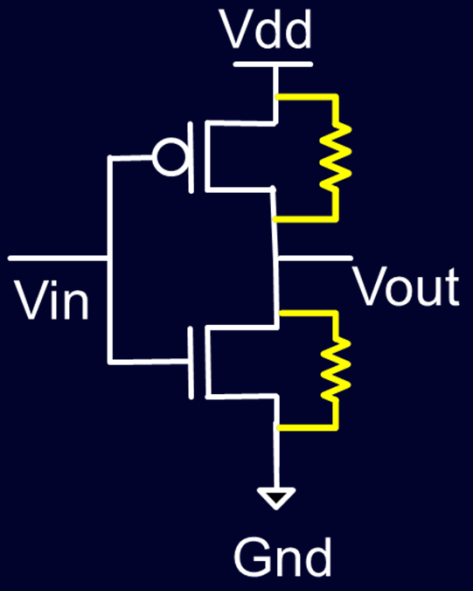
Ideal CNFET Inverter



CNFETs: BIG Promise, BUT

- Major barriers for a decade
  - Mis-positioned CNTs
  - Metallic CNTs
- Processing alone inadequate

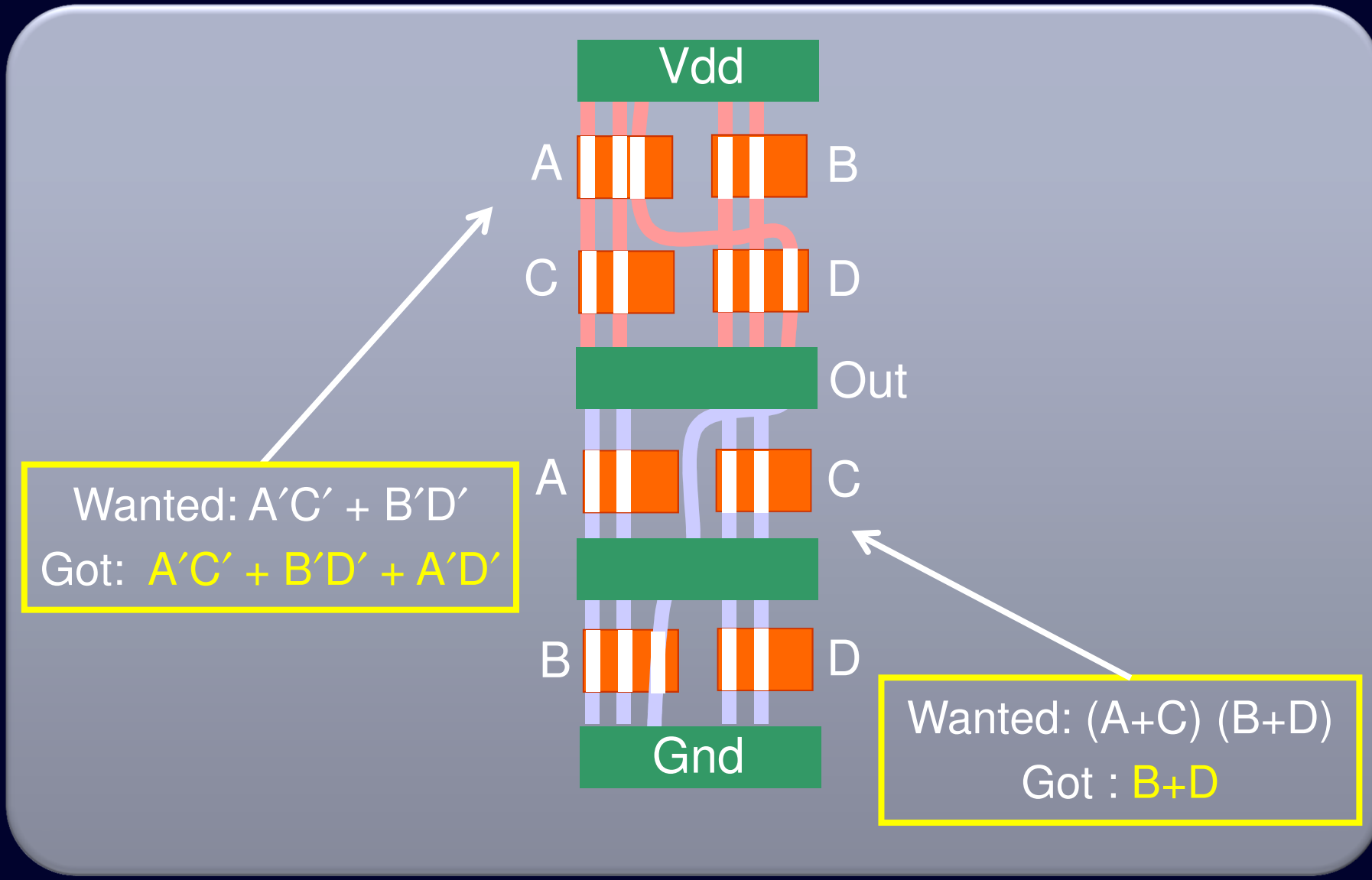




Imperfection-immune design essential

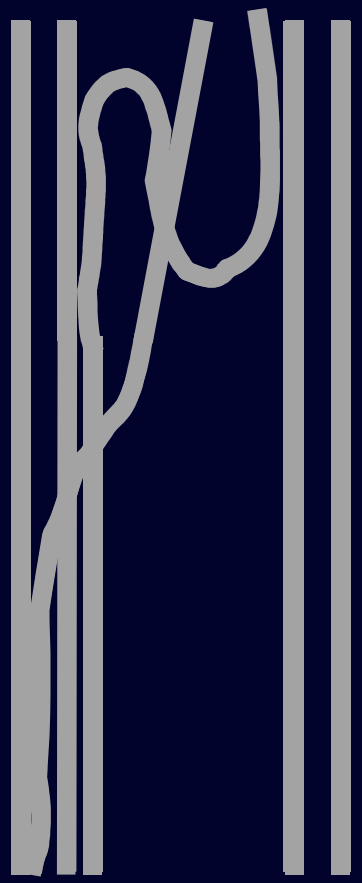
Collaborator: Prof. H.-S.P. Wong, Stanford

Mis-positioned CNTs: Incorrect Logic



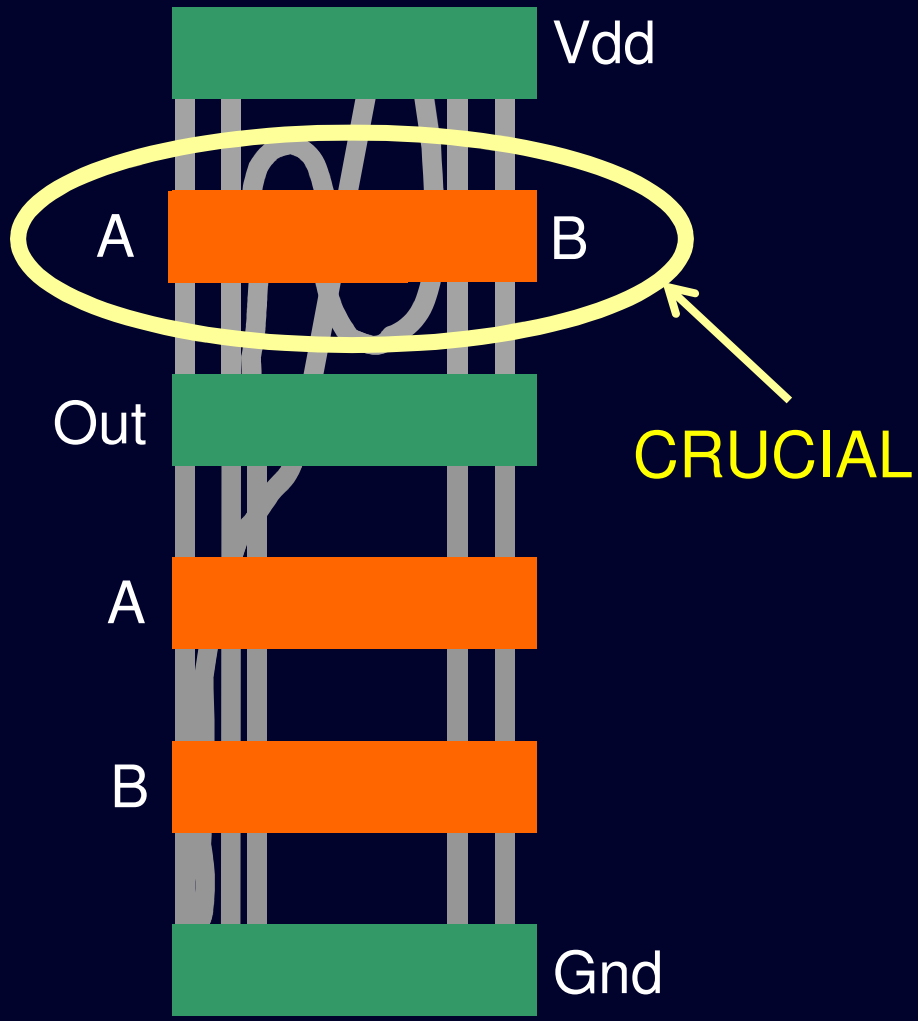
Mis-positioned-CNT-Immune NAND

1. Grow CNTs



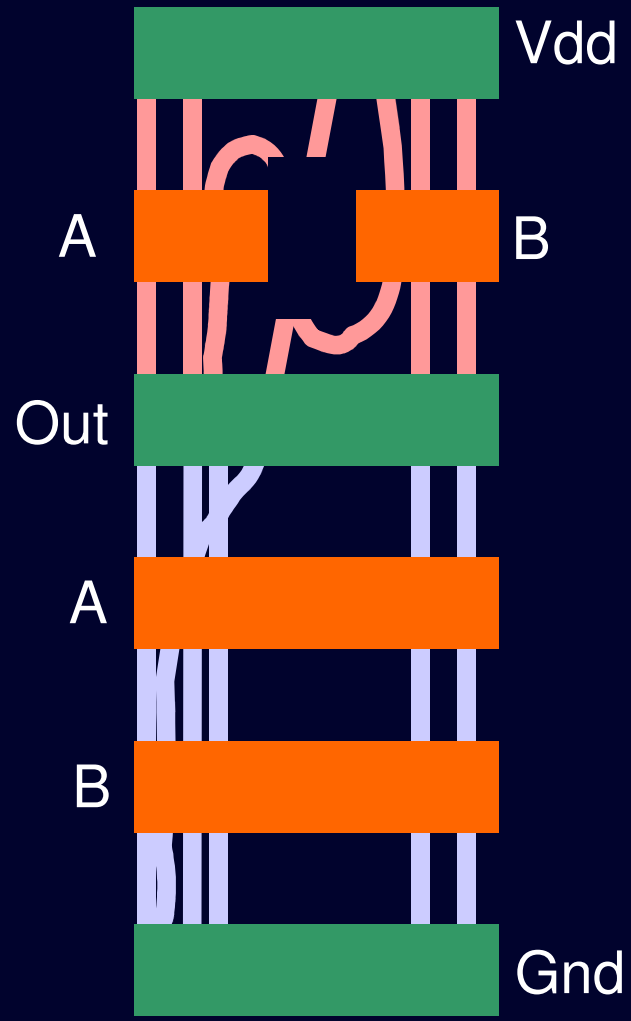
Mis-positioned-CNT-Immune NAND

1. Grow CNTs
2. Extended gate & contacts



Mis-positioned-CNT-Immune NAND

1. Grow CNTs
2. Extended gate & contacts
3. Etch gate & CNTs
4. Dope P & N regions



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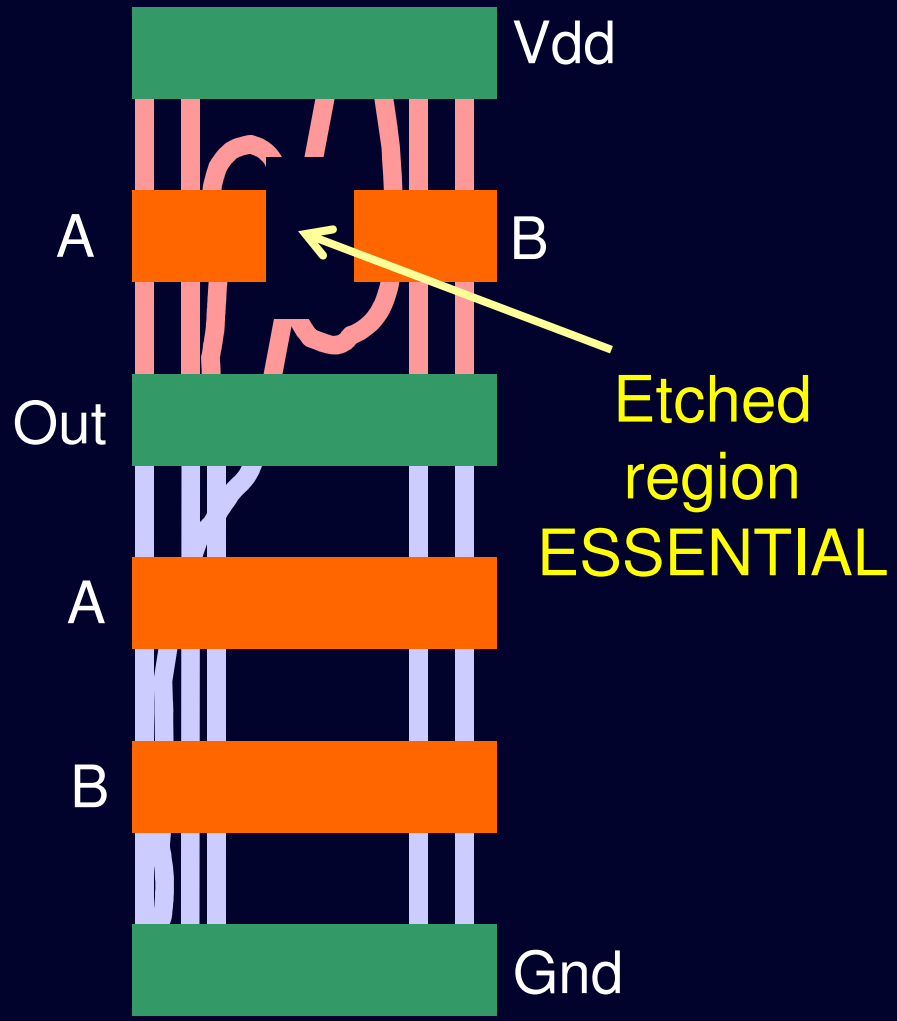

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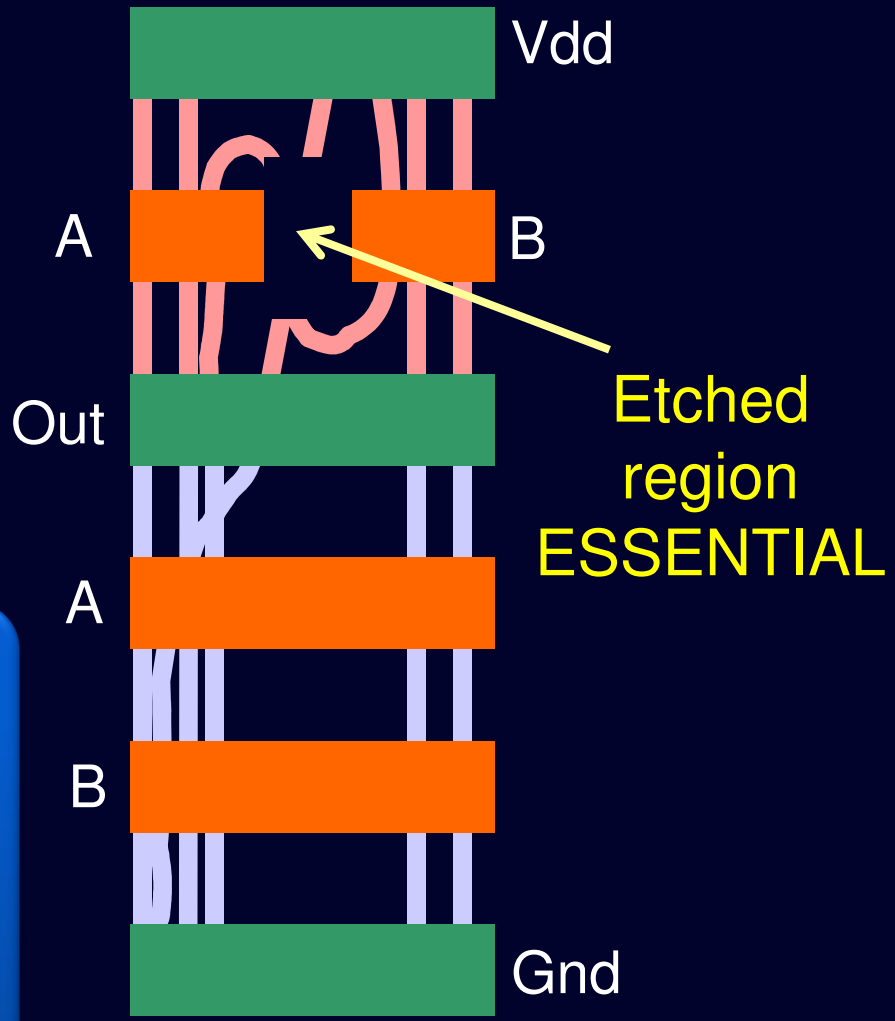
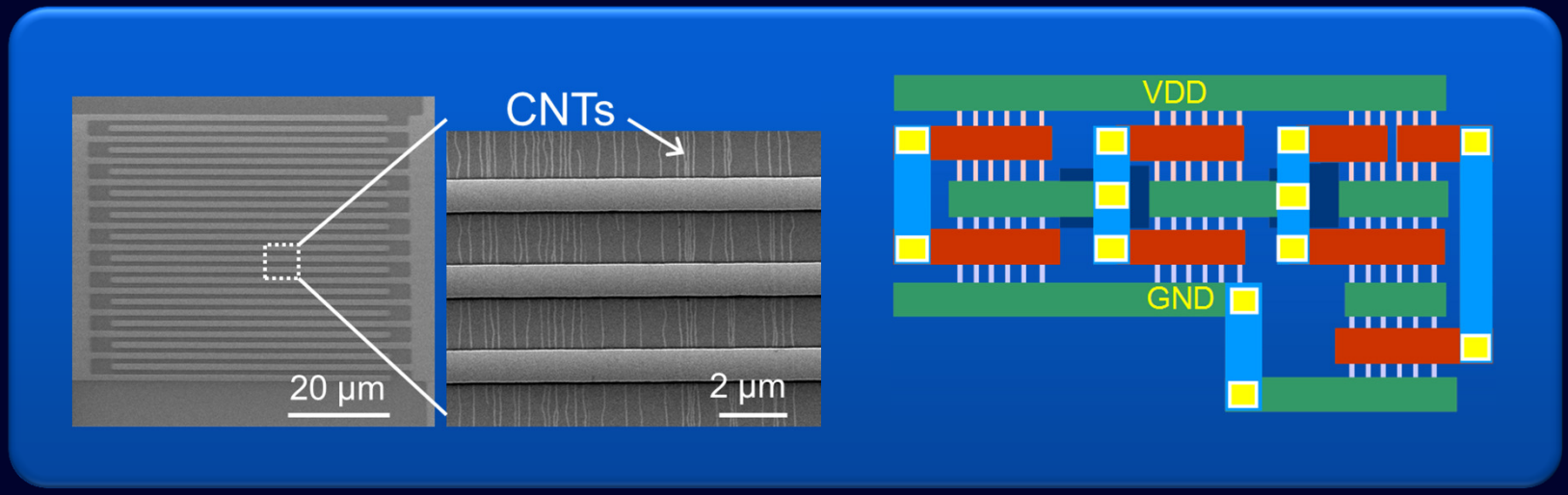


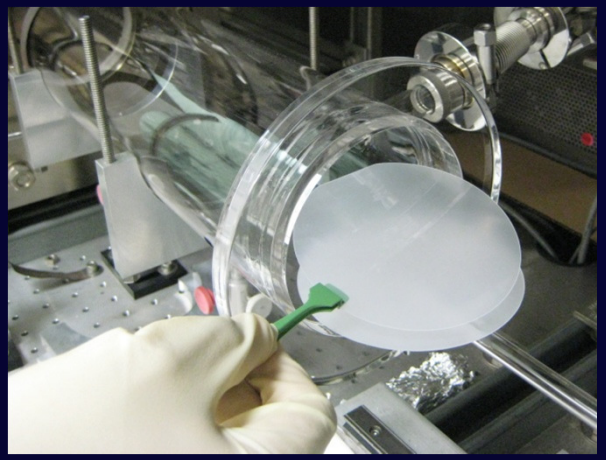
- Graph algorithms
  - All possible functions
- VLSI
  - Processing & design

VMR: VLSI Metallic CNT Removal

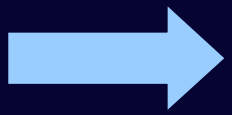
- Metallic-CNT-immune design
  - ☺ Sufficient: all possible logic designs
  - ☺ VLSI processing & design



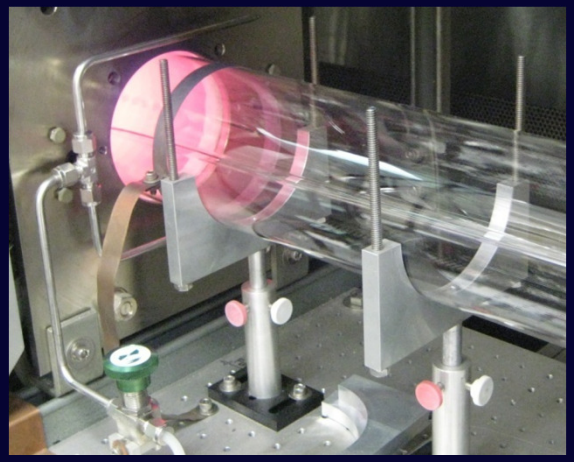
First Wafer-Scale Aligned CNT Growth



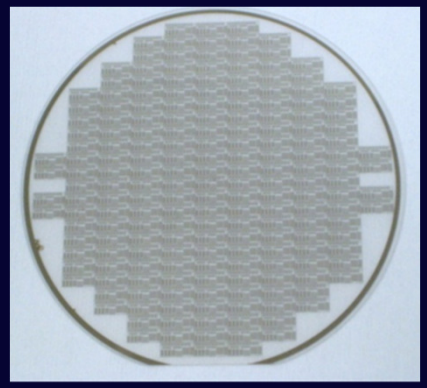
Quartz wafer
with catalyst



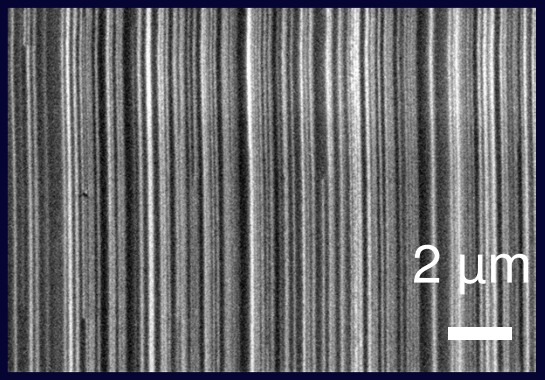
Aligned
CNT growth



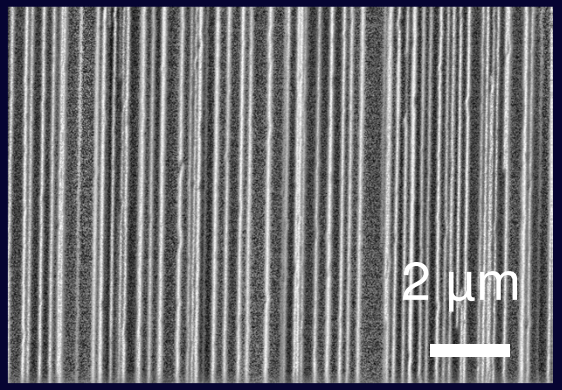
Quartz wafer
99.5% CNTs aligned



Before transfer
Quartz substrate

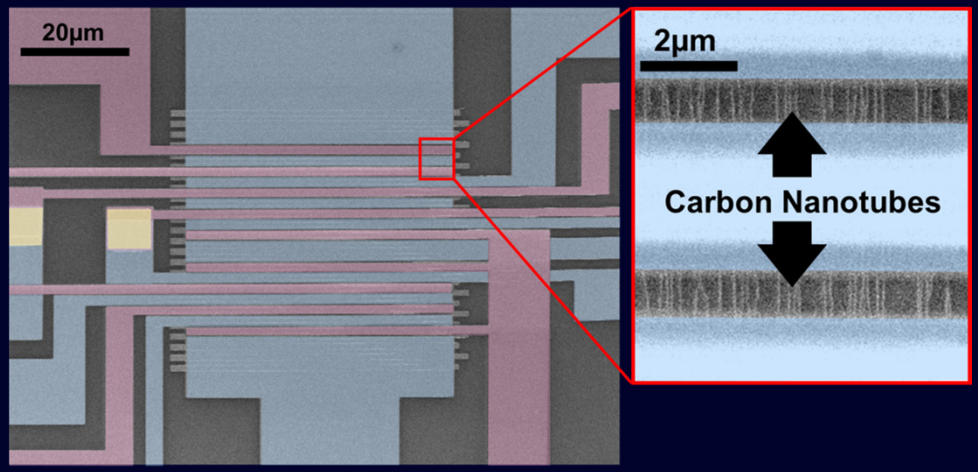


After transfer
SiO_2/Si substrate

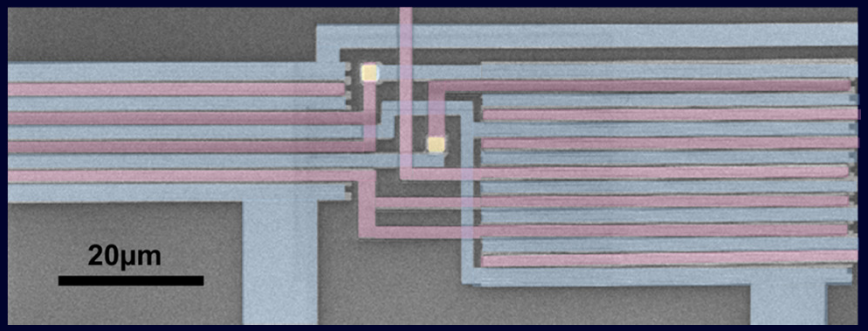


First Experimental Demonstrations

Imperfection-immune circuits
Arithmetic & storage

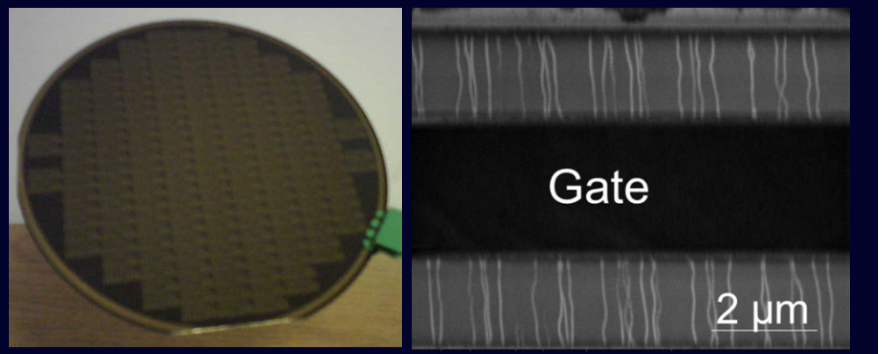


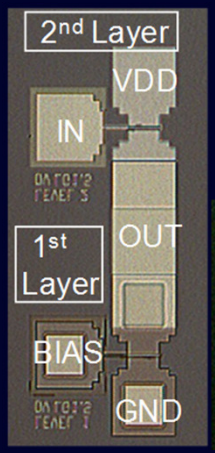
Adder sum



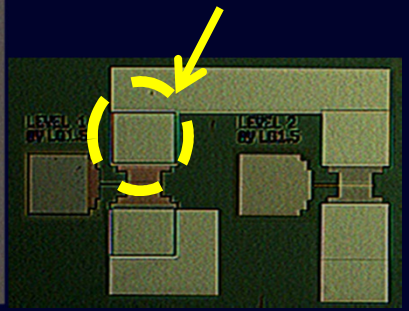
D-latch

VLSI Integration
Wafer-scale & monolithic 3D



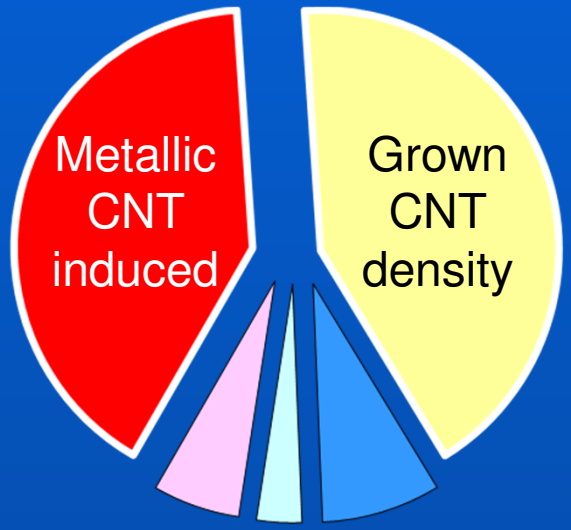


Conventional via, NOT TSV

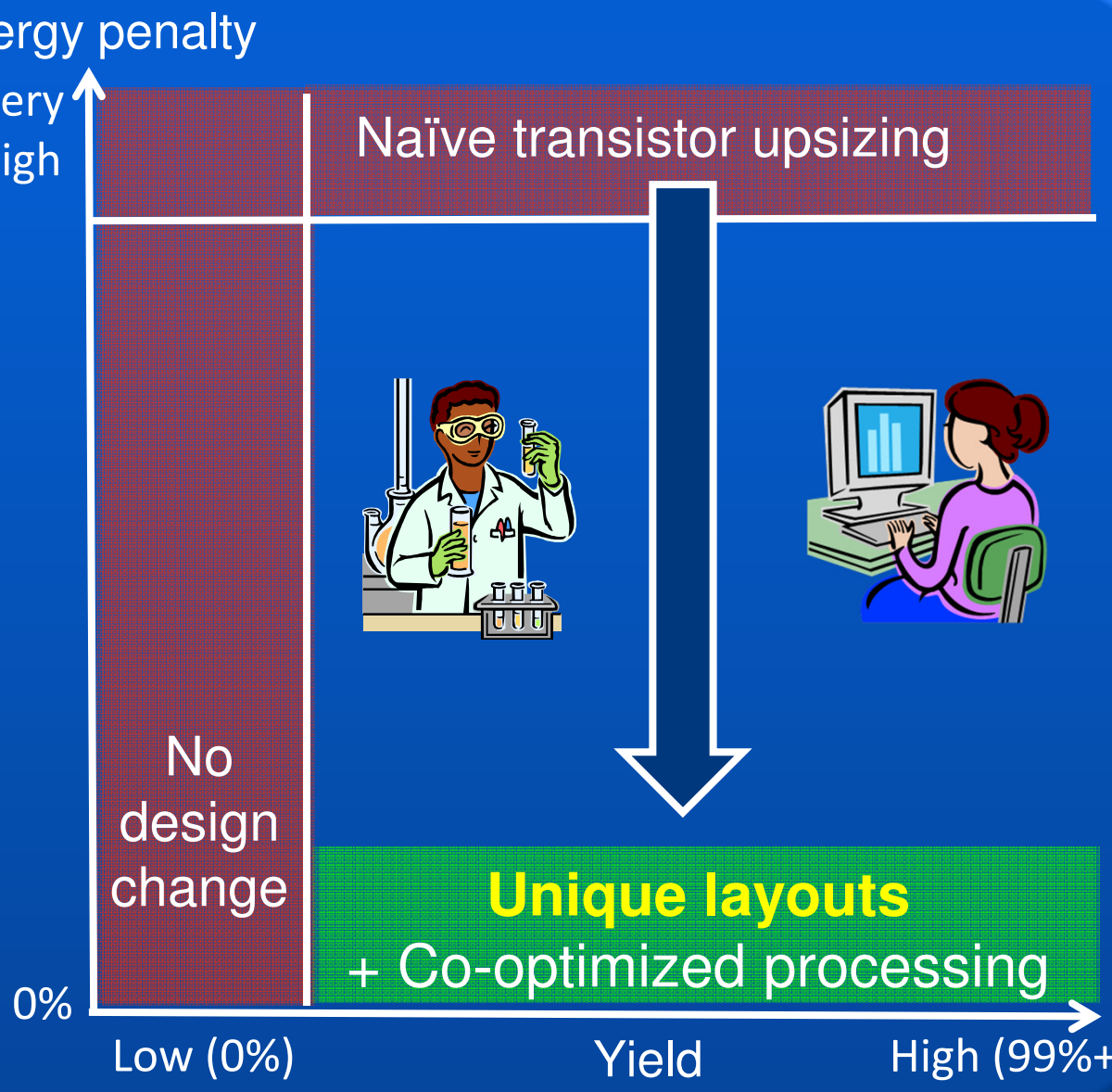


Multi-layer CNFET circuits

CNFET Variations Significant



CNFET I_{on} variations



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Thanks to my Research Group

Thanks to our Sponsors

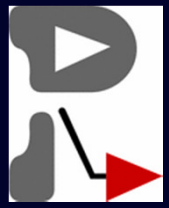


Photo credits:
Burn-in & test socket workshop, H. Dai, NEC, opensparc.net, Stanford

Concluding Remarks

- Derive failure signatures
- Utilize failure signatures
- Validate failure signatures

Enable

Nanotechnology Revolutions

&

A TRULY Better Tomorrow