

Low-cost Disaggregation of Sub-system Power



Yuwen Sun, Lucas Wanner, Puneet Gupta, and Mani Srivastava
UC Los Angeles

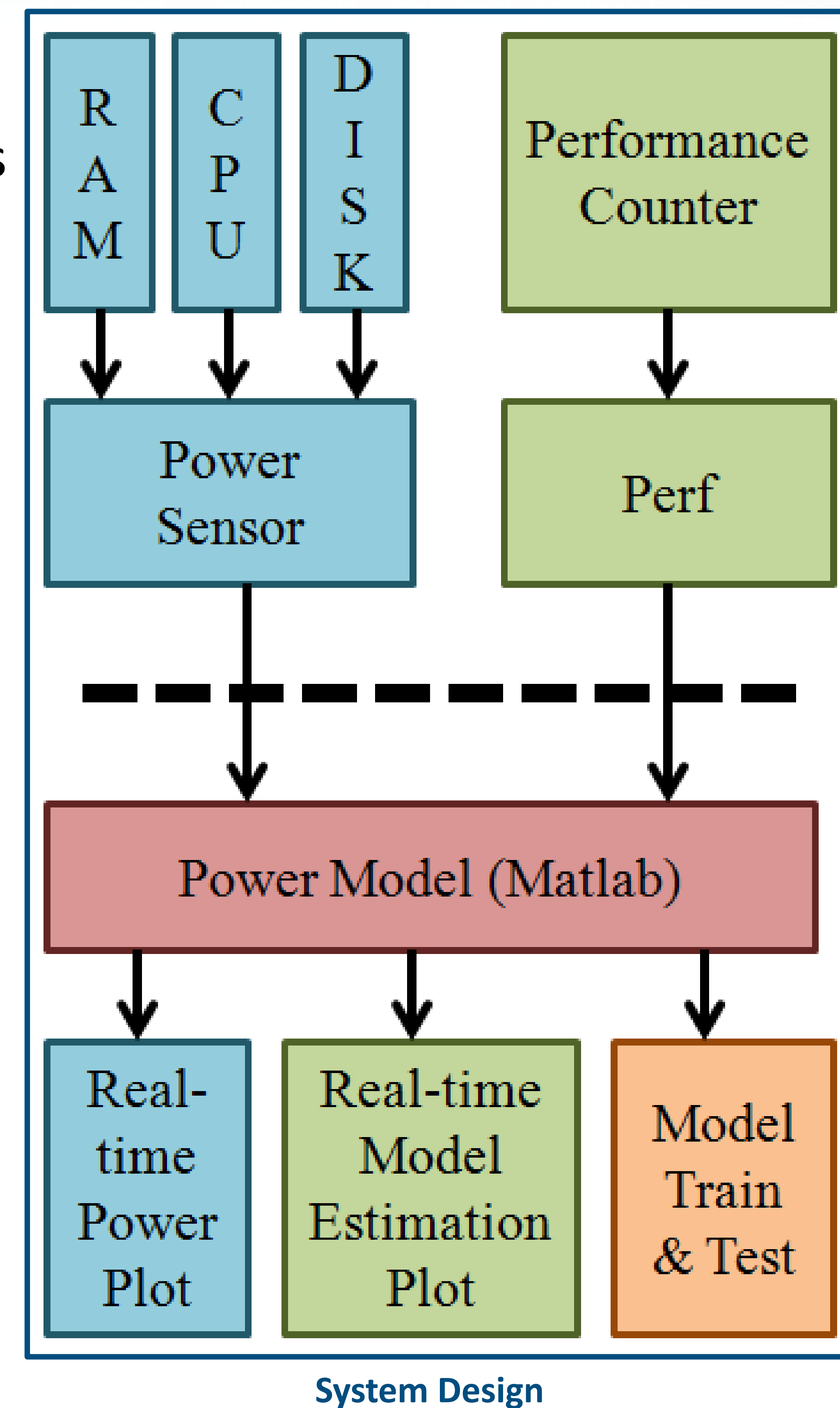


Motivation: sub-system power

- Fine-grained power info enables optimization & adaptation for OS and Apps
- Power sensors for each component in the system: simple, but expensive
- **Objective: sub-system power with only ONE system-wide power meter**

Approach: single power meter plus event counters

- Event counters record information about hardware usage: Context switches, cache misses, branches, etc.
- Hypothesis: **A linear model can predict sub-system power** using event counters and system-wide power info
- **Model: Low cost, transplantable, robust, and adaptable to variation**
Self-training cannot be achieved by traditional static model



Linear Model

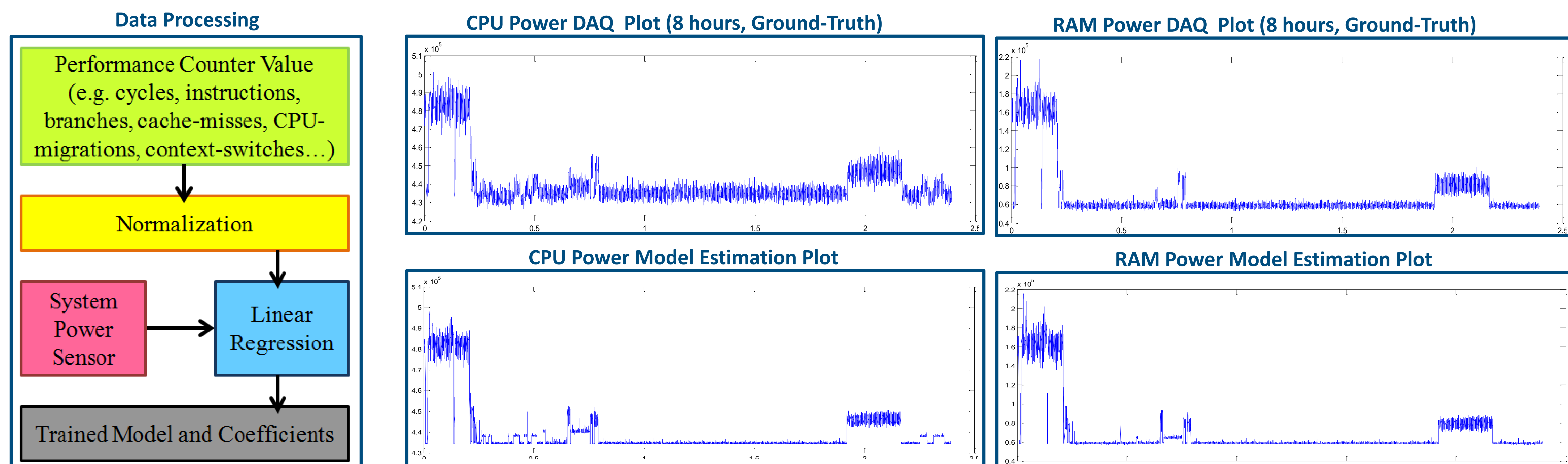
$$\text{Power}_{\text{Total}} = (\alpha \times \begin{pmatrix} C_{\text{RAM}1} \\ C_{\text{RAM}2} \\ \vdots \\ C_{\text{RAM}n} \end{pmatrix}^T + \beta \times \begin{pmatrix} C_{\text{CPU}1} \\ C_{\text{CPU}2} \\ \vdots \\ C_{\text{CPU}n} \end{pmatrix}^T + \gamma \times \begin{pmatrix} C_{\text{Disk}1} \\ C_{\text{Disk}2} \\ \vdots \\ C_{\text{disk}n} \end{pmatrix}^T) \times \begin{pmatrix} \text{Per-Counter 1} \\ \text{Per-Counter 2} \\ \vdots \\ \text{Per-Counter n} \end{pmatrix}$$

Preliminary Results

- Testbed: Sub-system power sensors as ground truth and system-wide power sensor as input to linear model
- Training: Ground truth power and event counters are recorded for CPU and Memory-intensive benchmarks
- **Testing: Real-time disaggregation of power with accuracy of 95%**
- **Live Demo**

Future Works

- Sophisticated model
- Different hardware/software information
- Various training algorithms & tools



NSF Expedition in Computing, Variability-Aware Software for Efficient Computing with Nanoscale Devices <http://variability.org>

